CLAIMS

What is claimed is:

1. A method comprising:

reading a performance information associated with a processor;

locating a processor performance table that corresponds to the performance information, the performance table including a plurality of performance parameters to control performance of the processor; and

updating a performance state (PS) structure using one of the processor performance table and a default table.

2. The method of claim 1 wherein reading the performance information comprises:

reading one of a maximum performance parameter and a minimum performance parameter from a register in the processor.

3. The method of claim 1 wherein locating the performance table comprises:

scanning through a set of performance tables;

comparing the performance information with performance indices in the performance tables; and

if at least one the performance indices matches with the performance information, copying entries of the processor performance table corresponding to the at least one of the performance indices to a local table, else copying the default table to the local table.

4. The method of claim 3 wherein updating the PS structure comprises:

parsing a source language code containing the PS structure; and

replacing entries in the PS structure by the local table.

5. The method of claim 1 further comprising:

updating a checksum for a description table according to an advanced configuration and power management (ACPI) protocol.

6. The method of claim 1 wherein reading the performance information comprises:

reading a bus ratio parameter and a voltage identifier, the bus ratio parameter corresponding to an operating frequency, the voltage identifier corresponding to an operating power of the processor.

7. A method comprising:

booting a platform having a processor after a performance state (PS) structure is updated;

loading an advanced configuration and power management (ACPI) operating system (OS); and

transitioning to a next performance state based on a performance criteria using the PS structure.

8. The method of claim 7 further comprises:

evaluating the PS structure.

9. The method of claim 7 wherein transitioning comprises:

reading a current performance information from a status register in a processor;

comparing the current performance information with the PS structure to locate a current entry in the PS structure; and

obtaining a next entry based on the current entry.

10. The method of claim 9 wherein transitioning further comprising:

updating a control register associated with performance of the processor using the next entry.

11. A computer program product comprises:

a machine useable medium having computer program code embedded therein, the computer program product having:

computer readable program code to read a performance information associated with a processor;

computer readable program code to locate a processor performance table that corresponds to the performance information, the performance table including a plurality of performance parameters to control performance of the processor; and

computer readable program code to update a performance state (PS) structure using one of the processor performance table and a default table.

12. The computer program product of claim 11 wherein the computer readable program code to read the performance information comprises:

computer readable program code to read one of a maximum performance parameter and a minimum performance parameter from a register in the processor.

13. The computer program product of claim 11 wherein the computer readable program code to locate the performance table comprises:

computer readable program code to scan through a set of performance tables;

computer readable program code to compare the performance information with performance indices in the performance tables;

computer readable program code to copy entries of the processor performance table corresponding to at least one of the performance indices to a local table if the at least one of the performance indices matches with the performance information, and

computer readable program code to copy the default table to the local table if none of the performance indices matches with the performance information.

14. The computer program product of claim 11 wherein the computer readable program code to update the PS structure comprises:

computer readable program code to parse a source language code containing the PS structure; and

computer readable program code to replace entries in the PS structure by the local table.

15. The computer program product of claim 11 further comprising:

computer readable program code to update a checksum for a description table according to an advanced configuration and power management (ACPI) protocol.

16. The computer program product of claim 11 wherein the computer readable program code to read the performance information comprises:

computer readable program code to read a bus ratio parameter and a voltage identifier, the bus ratio parameter corresponding to an operating frequency, the voltage identifier corresponding to an operating power of the processor.

17. A computer program product comprising:

a machine useable medium having computer program code embedded therein, the computer program product having:

computer readable program code to boot a platform having a processor after a performance state (PS) structure is updated;

computer readable program code to load an advanced configuration and power management (ACPI) operating system (OS); and

computer readable program code to transition to a next performance state based on a performance criteria using the PS structure.

18. The computer program product of claim 17 further comprises:

computer readable program code to evaluate the PS structure.

19. The computer program product of claim 17 wherein the computer readable program code to transition comprises:

computer readable program code to read a current performance information from a status register in a processor;

computer readable program code to compare the current performance information with the PS structure to locate a current entry in the PS structure; and

computer readable program code to obtain a next entry based on the current entry.

20. The computer program product of claim 19 wherein the computer readable program code to transition further comprising:

computer readable program code to update a control register associated with performance of the processor using the next entry.

21. A system comprising:

a processor;

a memory coupled to the host to store a system management interrupt (SMI) handler, the SMI handler when executed in response to an SMI, causing the processor to:

read a performance information associated with a processor,

locate a processor performance table that corresponds to the performance information, the performance table including a plurality of performance parameters to control performance of the processor, and

update a performance state (PS) structure using one of the processor performance table and a default table.

22. The system of claim 21 wherein the SMI handler causing the processor to read the performance information causes the processor to:

read one of a maximum performance parameter and a minimum performance parameter from a register in the processor.

23. The system of claim 21 wherein the SMI handler causing the processor to locate the performance table causes the processor to:

scan through a set of performance tables;

compare the performance information with performance indices in the performance tables; and

if at least one of the performance indices matches with the performance information, copy entries of the processor performance table corresponding to the at least one of the performance indices to a local table, else copy the default table to the local table.

24. The system of claim 21 wherein the SMI handler causing the processor to update the PS structure causes the processor to:

parse a source language code containing the PS structure; and

replace entries in the PS structure by the local table.

25. The system of claim 21 the SMI handler further causes the processor to:

update a checksum for a description table according to an advanced configuration and power management (ACPI) protocol.

26. The system of claim 21 wherein the SMI handler causing the processor to read the performance information causes the processor to:

read a bus ratio parameter and a voltage identifier, the bus ratio parameter corresponding to an operating frequency, the voltage identifier corresponding to an operating power of the processor.

27. A system comprising:

a processor in a platform;

a system memory coupled to the processor; and

a basic input output system (BIOS) memory coupled to the processor, the BIOS memory storing a system management interrupt (SMI) handler, the SMI handler, when executed in response to an SMI, causing the processor to:

boot the platform after a performance state (PS) structure is updated, and

load an advanced configuration and power management (ACPI) operating system (OS) into the system memory, the ACPI OS, when executed, causing the processor to transition to a next performance state based on a performance criteria using the PS structure.

28. The system of claim 27 wherein the ACPI OS, when executed, further causes the processor to:

evaluate the PS structure.

29. The system of claim 27 wherein the ACPI OS causing the processor to transition causes the processor to:

read a current performance information from a status register in the processor;

compare the current performance information with the PS structure to locate a current entry in the PS structure; and

obtain a next entry based on the current entry.

30. The system of claim 29 wherein the ACPI OS causing the processor to transition further causes the processor to:

update a control register associated with performance of the processor using the next entry.